PO 5/8/1883

NAVRIS
ACQUISITION CR SUMMARY

NAVRIS
24-FEB-06

Batch

CR NUMBER: 06PR03921-01

PREVIOUS CR NUMBER: 06PR03921-00

TITLE: DEVELOPMENT OF PROCESS TECHNOLOGIES FOR HIGH-PERFORMANCE MOS-BASED SIC POWER SWITCHING DEVICES

AWARD NUMBER: N000140510437 **SHORT CONTRACTOR CODE:** PRDW
NAVRIS NUMBER: 1012485 **UIC/CAGE CODE:** 6D418
MODIFICATION NUMBER: P00003
SIZE AND TYPE OF BUSINESS: NONPROFIT-EDUC./NOT HISTORICALLY BLACK/OTHER

PI NAME: COOPER, JAMES A
PERFORMER: PURDUE UNIVERSITY

PO NAME: MACK, INGHAM ARTHUR
PO CODE: 0312 **PO PHONE:** (703) 696-4825
POINT OF CONTACT: BROWN, STACY L **POC PHONE:**
GRANTS OFFICER: FORD, ELIZABETH

CURRENT AWARD START DATE: 01-MAR-05
CURRENT AWARD END DATE: 31-AUG-06
PO REQUESTED START DATE: 17-FEB-06

CR TYPE: INCREMENTAL FUNDING

INTERNAL COORDINATOR(S) **PHONE**
INSTRUMENT TYPE: GRANT
BASIS FOR SELECTION: BAA
CBD DATE: 24-FEB-06

CURRENT FUNDING:

ACRN	APPN	SBHD	OBJ	PARM	BCN	SA	AAA	TT	PAA	COSTCODE
AA	0400	1304	255	RA	RA313	0	068342	2D	000000	R5720000T972

BA	FY	FRC	PE	AMOUNT	STATUS	FUND SOURCE	OPTION
D	2005	A119	0602716E	$47,843.00	APPROVED	DARPA	NO

FUTURE FRC:

FY	FRC	START DATE	AMOUNT

CR STATUS: APPROVED

CUMULATIVE TOTAL AWARD VALUE: $2,467,843.00
TOTAL VALUE FOR CR: $47,843.00
INCREMENTAL VALUE: $47,843.00
MODIFICATION NEGOTIATED VALUE: $47,843.00

OK Eric 3/13/06

Error message

Requisition Number
3070601

NOTES:

Short Work Statement
Funds are provided to control and stablize the threshold voltage of IGBTs, grow thick epilayers that can suport 15- 25 kV, and design, fabricate, and characterize SiC IGBTs for the 15 - 25kV regime.

Notes to Acquisition
The design of test chips for both n-channel and p-channel IGBTs has been completed and photomasks have been made. Growth conditions that produce 200 um n-type 4H-SiC blocking layers with good surface morphology and controllable doping in the 1 - 3e14 cm-3 range, as needed for 20 kV n-channel IGBT devices have been established. One of epilayers, with a thickness of 182 um and doping of 1e14 cm-3 was sent to NovaSiC for substrate removal. Experiments have been conducted to assess the efficacy of oxidation or post-oxidation annealing in an alumina environment.
additonal funds sent by DARPA

FY05 Funds

INRIS
PR SUMMARY REPORT

CARROLV / PRODUCT
08-DEC-2005
06PR03921-00

PR Number: 06PR03921-00

Previous PR Number: 304809
Title: Development of Process Technologies for High-Performance MOS-Based SiC Power Switching Devices

Award Number: N000140510437
Modification Number: P00002

Short Contractor Code: prdw
Size and Type of Business: 1p Nonprofit-Educ./Not Historically Black/Other

P.I. Name: James Cooper
Performer: PURDUE UNIVERSITY
302 WOOD ST YOUNG HALL
WEST LAFAYETTE, IN 479072108

P.O. Name: Ingham Mack
P.O. Code: 312
P.O. Phone: (703) 696-4825
Point of Contact: Brown Stacy
Phone: (765) 494-1619
Grants Officer:

Current Award Start Date: 01-MAR-05
Current Award End Date: 31-AUG-06
P.O. Requested Start Date: 15-DEC-05
P.O. Requested End Date: 31-AUG-06

PR Type: Incremental Funding

Internal Coordinator(s):
Phone:

Li2

Instrument Type: Grant
Basis For Selection: (baa)
CBD Date:

Current Funding:

ACRN	APPN	SBHD	OBJ	PA RM	BCN	SA	AAA	TT	PAA	COST CODE	AMOU
AA	9750400	1304	000	RA 31	3	068342	2D	000000	R5720000	T972	$820,000.0(

FRC: A119 Expiration: 30-SEP-06

Future Funding:

FY	FRC	NEG	START DATE	AMOUNT
2006	TBD		01-OCT-05	$ 47,843.00

PR Status: Committed

Equipment Cost (Current Year): $ 0.00

Cumulative Total Award Value:	$ 2,467,843.00
Total Value of PR:	$ 820,000.00
Increment Value:	$ 820,000.00
Modification Negotiated Value:	$ 0.00

Short Work Statement

Funds are provided to control and stablize the threshold voltage of IGBTs, grow thick epilayers that can suport 15- 25 kV, and design, fabricate, and characterize SiC IGBTs for the 15 - 25kV regime.

PR Number: 05PR07240-01

Previous PR Number: 304809
Title: Development of Process Technologies for High-Performance MOS-Based SiC Power Switching Devices

Award Number: N000140510437
Modification Number: P00001

Short Contractor Code: prdw
Size and Type of Business: 1p
Nonprofit-Educ./Not Historically Black/Other

P.I. Name: James Cooper
Performer: PURDUE UNIVERSITY
302 WOOD ST YOUNG HALL
WEST LAFAYETTE, IN 479072108

P.O. Name: Ingham Mack
P.O. Code: 312
Point of Contact: Brown Stacy
Grants Officer:

P.O. Phone: (703) 696-4825
Phone: (765) 494-1619

Current Award Start Date: 01-MAR-05
Current Award End Date: 31-AUG-06
P.O. Requested Start Date: 15-AUG-05
P.O. Requested End Date: 31-AUG-06

PR Type: Incremental Funding

Internal Coordinator(s):

Phone:

Carol
6.2 funds

Instrument Type: Grant
Basis For Selection: (baa)
CBD Date:

Current Funding:

ACRN	APPN	SBHD	OBJ	PA RM	BCN	SA	AAA	TT	PAA	COST CODE	AMOUNT
AA	9750400	1304	000	RA 31	3	068342	2D	000000	R5720000	T972	$80,000.00

FRC: A119 Expiration: 30-SEP-05

Future Funding:

FY	FRC	NEG START DATE	AMOUNT
2006	TBD	01-OCT-05	$ 867,843.00

PR Status: Committed

Equipment Cost (Current Year): $ 0.00

Cumulative Total Award Value:	$ 1,600,000.00
Total Value of PR:	$ 80,000.00
Increment Value:	$ 80,000.00
Modification Negotiated Value:	$ -671,902.82

Short Work Statement

Funds are provided to control and stablize the threshold voltage of IGBTs, grow thick epilayers that can suport 15- 25 kV, and design, fabricate, and characterize SiC IGBTs for the 15 - 25kV regime.

PR Number: 05PR07240-00

Previous PR Number:
Title: Wide Bandgap Semiconductor High Power Electronics

Award Number: N000140510437
Modification Number:

Short Contractor Code: prdw
Size and Type of Business: 1p
Nonprofit-Educ./Not Historically Black/Other

P.I. Name: James Cooper
Performer: PURDUE UNIVERSITY
1063 HOVDE HALL
WEST LAFAYETTE, IN 479071063

P.O. Name: Ingham Mack
P.O. Code: 312
P.O. Phone: (703) 696-4825
Point of Contact:
Phone:
Grants Officer:

Current Award Start Date: 01-MAR-05
Current Award End Date: 31-AUG-06
P.O. Requested Start Date: 01-MAR-05
P.O. Requested End Date: 31-AUG-06

Carol

PR Type: New

Internal Coordinator(s):
Phone:

Instrument Type: Grant
Basis For Selection: (baa)
CBD Date: 08-SEP-04

Current Funding:

ACRN	APPN	SBHD	OBJ	PA RM	BCN	SA	AAA	TT	PAA	COST CODE	AMOU
AA	9750400	1304	000	RA 31	3	068342	2D	000000	R5720000	T972	$1,520,000.00

FRC: A119 Expiration: 30-SEP-05

Future Funding:

FY	FRC	NEG	START DATE	AMOUNT

PR Status: Approved (Active)

Equipment Cost (Current Year): $ 0.00

6.2 funds

Cumulative Total Award Value:	$ 1,520,000.00
Total Value of PR:	$ 1,520,000.00
Increment Value:	$ 1,520,000.00
Modification Negotiated Value:	$11,503,087.00

Short Work Statement

Funds are provided to control and stablize the threshold voltage of IGBTs, grow thick epilayers that can suport 15- 25 kV, and design, fabricate, and characterize SiC IGBTs for the 15 - 25kV regime.

BPS: Submission, Evaluation, Cost

This proposal was received and evaluated in accordance with The DARPA BAA for WBG High Power Electronics 04-28. Award is recommended based on evaluation of the proposal (provided separately) in accordance with the criteria stated in the announcement/solicitation.

Financial Considerations:
Labor -

The proposed quantities and types of labor (including any consultants and labor provided by subgrantee) are reasonable and necessary for accomplishing the research project.

The proposed labor rates are in line with standard academic or industrial practice for research of this type.

Any consulting at a rate in excess of $500.00 per day is justified in the "Additional Consultant Information" text item.

Other Direct Costs-

Other proposed direct costs (such as supplies, equipment, ADP, travel, etc.) are reasonable and necessary for accomplishing the research project.

I have reviewed and accepted the proposed budget subject to the grant/contracting officer's verification of rates in indirect costs. Where changes to the original budget were necessary I have had the principal investigator submit a revised budget through official university channels and that revised budget is enclosed. The proposal appears to be fair, reasonable, in the interest of the government, and is consistent with other previous and current efforts of this nature.

BPS: Overall Merits

This program will address the needs for implementing a Solid State Power Substation that can be used on navy surface combatants to reduce the size and weight of current systems.

BPS: ONR Mission

This program will address the need to reduce the size and increase the performance of high power electrical control and conversion systems for naval surface combatants.

BPS: Contractor Qualifications

The members of this team are well qualified to perform the tasks as presented in the proposal. Purdue has experience in SiC devices and applications while other members of the team are known for materials and device characterization as well as process development. All contractors have the facilities to perform the proposed work.

BPS: PI Qualifications

Dr. Cooper has worked in the field of device electronics for 31 years. He is the author/co-author of over 200 technical publications and conference presentations and holds 11 U.S. patents. Dr. Cooper is a recognized leader in the area of power semiconductor devices.

PR Number: 05PR07240-00 Unclassified

CLEARANCE MEMORANDUM
GRANTS WITH EDUCATIONAL AND NONPROFIT INSTITUTIONS

GRANTEE: PURDUE UNIVERSITY
SPONSORED PROGRAM SERVICES
302 WOOD ST YOUNG HALL
WEST LAFAYETTE, IN 47907-2040

GRANT NO: N00014-05-1-0437

AUTHORITY: 10 USC 2358, as amended, and 31 U.S.C. 6304.

1. Selection Procedure: Broad Agency Announcement

This proposal was received in response to the ONRannouncement of research interest published in the COMMERCE BUSINESS DAILY of 08 SEP 04. The Program Officer recommends award based on evaluation of the proposal in accordance with the criteria set forth in the announcement.

2. Proposal Identification.

Title:	Development of Process Technologies for High-Performance MOS-Based SiC Power Switching Devices
Number:	N/A
Date:	31 AUG 04
As revised:	N/A

3. Principal Investigator: James A. Cooper

4. Document type: Domestic Research Grant

5. Description of Work: The Grantee's proposed work description is incorporated in the Grant by reference.

6. Analysis of Cost/Price:

A copy of the proposed budget is attached.

a. The Program Officer has reviewed the quantities and types of labor, including consultants and subgrantee labor, and also the other direct cost items (such as travel, equipment, supplies, materials, ADP, etc.) and has determined them to be appropriate for the proposed research.

b. The Specialist has reviewed the budget and determined that the other direct cost items are acceptable.

See justification in back-up file.

c. The Specialist has reviewed the proposed indirect costs as noted below:

(1) Fringe Benefit Rate: The proposed rate(s) is/are in accordance with current fixed rates or prospective forward pricing rate(s) and is/are correctly applied to the proper base.

(2) Indirect Cost Rate: The Grantee has proposed indirect costs which are in accordance with current policies or as prospectively agreed to until a future negotiation agreement takes effect. The rate(s) is/are correctly applied to the proper base.

7. Other Negotiated Terms and Conditions:

a. Negotiated Grant Value: $ 2,467,843.00
Increment Value: $ 1,520,000.00
Period covered by increment: 01 MAR 05 to 30 SEP 05

b. Period of Performance: 01 MAR 05 to 31 AUG 06

8. Certifications:

The appropriate certifications have been submitted by the Grantee and are located in the grant file.

COORDINATED WITH: Stacy L. Brown
PHONE: (765) 494-3514

9. Reasonableness:

In the opinion of the undersigned, the terms and conditions of this action appear to be fair, reasonable, and in the best interests of the Government.

(b) (6)

Carol A. Porter	14 MAR 05	ONR 251	(703) 696-2587
GRANT NEGOTIATOR	DATE	CODE	TELEPHONE NUMBER

CONTRACT COMPLETION STATEMENT

1. FROM: *(Award Administration Office)*

Office of Naval Research, Chicago Regional Office
230 S. Dearborn
Room 380
Chicago, IL 60604-1595
Main Office (312) 886-5423Â Â Â Â FAX:(312) 353-2094

2a. AWARD NUMBER
N000140510437

2b. LAST ADMINISTATION MODIFICATION NUMBER
A00002

2c. LAST AWARDING AGENCY MODIFICATION NUMBER
P00003

3: TO: *(Name and Address of Awarding Agency or Payment office, as applicable)*

Â Â
OFFICE OF NAVAL RESEARCH
875 NORTH RANDOLPH STREET
ATTN: BD25 - Mail Room
ARLINGTONÂ VAÂ 22203-1995

4. NAME OF AWARDEE
Purdue University
West Lafayette, IN

5. EXCESS FUNDS (ULO)
$0.00

6a. IF FINAL PAYMENT HAS BEEN MADE, COMPLETE ITMES 6b., and 6c.	6b. VOUCHER NUMBER	6c. DATE
	018	10/18/2007
7a. IF FINAL APPROVED INVOICE FORWARDED TO D.O. OF ANOTHER ACTIVITY AND STATUS OF PAYMENT IS UNKNOWN, COMPLETE ITEMS 7b., AND 7c.	**7b. INVOICE NUMBER**	**7c. DATE FORWARDED**

8. REMARKS

	CAMIS	STARS
Total amount obligated:	$2,461,887.45	$2,461,887.45
Total amount approved/disbursed:	$2,461,887.45	$2,461,887.45
Excess funds to deobligate (ULO):	$0.00	$0.00

9a. ALL ADMINISTRATION OFFICE ACTIONS REQUIRED HAVE BEEN SATISFACTORILY COMPLETED. THIS INCLUDES FINAL SETTLEMENT IN THE CASE OF A PRICE REVISION CONTRACT

9b. TYPED NAME OF RESPONSIBLE OFFICIAL	9c. SIGNATURE	9d. DATE
John Chiappe Administrative Contracting Officer	(b) (6)	07/28/2010

FOR PURCHASING OFFICE USE ONLY

10a. ALL PURCHASING OFFICE ACTIONS REQUIRED HAVE BEEN FULLY AND SATISFACTORILY ACCOMPLISHED. AWARD FILE OF THIS OFFICE IS HEREBY CLOSED AS OF:

☒ DATE SHOWN IN ITEM 9d ABOVE

☐ DATE SHOWN IN ITEM 10e BELOW. (Check this box only if final completion of any significant purchasing office action extends more than three months beyond close-out date shown in item 9d. above. In such cases, submit a copy of the completed form upon final accomplishment of all purchasing office actions to the award administration office. (Upon receipt, the award administration office shall extend its contract file close-out date accordingly.))

10b. REMARKS

10c. TYPED NAME OF RESPONSIBLE OFFICIAL	10d. SIGNATURE	10e. DATE
Ellen Simonoff Contracting Officer	(b) (6)	AUG 07 2010

Central Contractor Registration

Advanced Search Information

Search Again | Print Record

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General Information

Current Registration Status: **Active in CCR; Registration valid until 09/27/2006.**

DUNS:	**072051394**
DUNS PLUS4:	
CAGE/NCAGE Code:	**6D418**
Legal Business Name:	**PURDUE UNIVERSITY**
Doing Business As (DBA):	
Division Name:	
Division Number	
Company URL:	

Physical Street Address 1:	**401 S GRANT ST**
Physical Street Address 2:	
Physical City:	**WEST LAFAYETTE**
Physical State:	**IN**
Physical Zip/Postal Code:	**47907-2024**
Physical Country:	**USA**

Mailing Name:	**PURDUE UNIVERSITY**
Mailing Address:	**SPONSORED PROGRAM SERVICES**
Mailing Address 2:	**302 WOOD ST. (YOUNG HALL)**
Mailing City:	**WEST LAFAYETTE**
Mailing State:	**IN**
Mailing Zip/Postal Code:	**47907-2108**
Mailing Country:	**USA**

Business Start Date: **07/02/1862**

Corporate Information

Type of Organization

Corporate Entity, Tax Exempt
(State of Incorporation is IN)

Business Types/Grants

A8 - Nonprofit Organization
G6 - 1862 Land Grant College
M8 - Educational Institution
VW - Contracts and Grants

Goods / Services

North American Industry Classification System (NAICS)

611310 COLLEGES, UNIVERSITIES, AND PROFESSIONAL SCHOOLS

Standard Industrial Classification (SIC)

8221 COLLEGES AND UNIVERSITIES

Product Service Codes (PSC)

-

Federal Supply Classification (FSC)

-

Small Business Types

This information comes from the Small Business Administration and is not editable by CCR vendors.

Business Types	Expiration Date
-	

North American Industry Classification System (NAICS)

NAICS Code	Description	Small Business	Emerging Small Business
611310	COLLEGES, UNIVERSITIES, AND PROFESSIONAL SCHOOLS	No	No

Points of Contact

Government Business POC Primary

Name:	MIKE LUDWIG
Address Line 1:	PURDUE UNIVERSITY
Address Line 2:	610 PURDUE MALL
City:	WEST LAFAYETTE
State:	IN
Zip/Postal Code:	479072040
Country:	USA
U.S. Phone:	Ext:
Non-U.S. Phone:	7654941063
Fax:	(765) 494-1360

Government Business POC Alternate

Name:	REBECCA L. WHITE
Address Line 1:	PURDUE UNIVERSITY
Address Line 2:	302 WOOD ST. (YOUNG HALL)
City:	WEST LAFAYETTE
State:	IN
Zip/Postal Code:	479072108
Country:	USA
U.S. Phone:	(765) 494-1052 Ext:
Non-U.S. Phone:	
Fax:	(765) 494-1360

Past Performance POC Primary

Name:	
Address Line 1:	
Address Line 2:	
City:	
State:	
Zip/Postal Code:	
Country:	
U.S. Phone:	Ext:
Non-U.S. Phone:	
Fax:	

Past Performance POC Alternate

Name:	
Address Line 1:	
Address Line 2:	
City:	
State:	
Zip/Postal Code:	
Country:	
U.S. Phone:	Ext:
Non-U.S. Phone:	
Fax:	

Electronic Business POC Primary

Name:	MIKE LUDWIG
Address Line 1:	PURDUE UNIVERSITY
Address Line 2:	610 PURDUE MALL
City:	WEST LAFAYETTE
State:	IN
Zip/Postal Code:	479072040
Country:	USA
U.S. Phone:	(765) 494-1063 Ext:
Non-U.S. Phone:	
Fax:	(765) 494-1360

Electronic Business POC Alternate

Name:	CAROLE PERIGO
Address Line 1:	PURDUE UNIVERSITY
Address Line 2:	610 PURDUE MALL - BURSAR OFFICE
City:	WEST LAFAYETTE
State:	IN
Zip/Postal Code:	479072040
Country:	USA
U.S. Phone:	(765) 494-1024 Ext:
Non-U.S. Phone:	
Fax:	(765) 494-3315

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

AUGUST 12, 2011

PTAS

103630377A

CAROL PETROSKY
OFFICE OF NAVAL RESEARCH
OFFICE COUNSEL
875 NORTH RANDOLPH STREET
ARLINGTON, VA 22203-1995

UNITED STATES PATENT AND TRADEMARK OFFICE
NOTICE OF RECORDATION OF ASSIGNMENT DOCUMENT

THE ENCLOSED DOCUMENT HAS BEEN RECORDED BY THE ASSIGNMENT DIVISION OF THE U.S. PATENT AND TRADEMARK OFFICE. A COMPLETE MICROFILM COPY IS AVAILABLE AT THE ASSIGNMENT SEARCH ROOM ON THE REEL AND FRAME NUMBER REFERENCED BELOW.

PLEASE REVIEW ALL INFORMATION CONTAINED ON THIS NOTICE. THE INFORMATION CONTAINED ON THIS RECORDATION NOTICE REFLECTS THE DATA PRESENT IN THE PATENT AND TRADEMARK ASSIGNMENT SYSTEM. IF YOU SHOULD FIND ANY ERRORS OR HAVE QUESTIONS CONCERNING THIS NOTICE, YOU MAY CONTACT THE EMPLOYEE WHOSE NAME APPEARS ON THIS NOTICE AT 571-272-3350. PLEASE SEND REQUEST FOR CORRECTION TO: U.S. PATENT AND TRADEMARK OFFICE, MAIL STOP: ASSIGNMENT SERVICES BRANCH, P.O. BOX 1450, ALEXANDRIA, VA 22313.

RECORDATION DATE: 08/08/2011

REEL/FRAME: 026740/0763
NUMBER OF PAGES: 2

BRIEF: CONFIRMATORY LICENSE (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
PURDUE UNIVERSITY

DOC DATE: 07/07/2006

ASSIGNEE:
NAVY, SECRETARY OF THE UNITED
STATES OF AMERICA
OFFICE OF NAVAL RESEARCH
875 NORTH RANDOLPH STREET
ARLINGTON, VIRGINIA 22203-1995

298-12-0001

APPLICATION NUMBER: 11338007 FILING DATE: 01/23/2006
PATENT NUMBER: 7498633 ISSUE DATE: 03/03/2009
TITLE: HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE

TONYA LEE, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

08/08/2011

Form PTO-1595 (Rev. 03-09)
OMB No. 0651-0027 (exp. 03/31/2009)

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

103630377

ET

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies)

PURDUE UNIVERSITY

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)

Name: NAVY, SECRETARY OF THE UNITED STATES

Internal Address: OF AMERICA

OFFICE OF NAVAL RESEARCH

Street Address: 875 NORTH RANDOLPH STREET

City: ARLINGTON

State: VA

Country: USA Zip: 22203-1995

Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance/Execution Date(s):

Execution Date(s) 07/07/2006

☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☒ Executive Order 9424, Confirmatory License
☐ Other

4. Application or patent number(s):

☐ This document is being filed together with a new application.

A. Patent Application No.(s)

11/338,007

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☒ No

Assignment Recordation Branch
Received
AUG - 8 2011
5th Floor
Public Records Division

5. Name and address to whom correspondence concerning document should be mailed:

Name: CAROL PETROSKY

Internal Address: OFFICE OF NAVAL RESEARCH

OFFICE OF COUNSEL

Street Address: 875 NORTH RANDOLPH STREET

City: ARLINGTON

State: VA Zip: 22203-1995

Phone Number: 703-696-4008

Fax Number: 703-696-6909

Email Address: CAROL.PETROSKY@NAVY.MIL

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 1.21(h) & 3.41) $

☐ Authorized to be charged to deposit account
☐ Enclosed
☒ None required (government interest not affecting title)

8. Payment Information

Deposit Account Number

Authorized User Name

9. Signature:

(b) (6) [redacted]

07/19/2011
Date

CAROL PETROSKY
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 2

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

Form PTO-1595 (Rev. 03-09)
OMB No. 0651-0027 (exp. 03/31/2009)

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

RECORDATION FORM COVER SHEET
PATENTS ONLY

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1. Name of conveying party(ies)

PURDUE UNIVERSITY

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)

Name: NAVY, SECRETARY OF THE UNITED STATES
Internal Address: OF AMERICA
OFFICE OF NAVAL RESEARCH
Street Address: 875 NORTH RANDOLPH STREET
City: ARLINGTON
State: VA
Country: USA Zip: 22203-1995

Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance/Execution Date(s):

Execution Date(s) 07/07/2006

☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☒ Executive Order 9424, Confirmatory License
☐ Other

4. Application or patent number(s):

☐ This document is being filed together with a new application.

A. Patent Application No.(s)

11/338,007

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☒ No

5. Name and address to whom correspondence concerning document should be mailed:

Name: CAROL PETROSKY
Internal Address: OFFICE OF NAVAL RESEARCH
OFFICE OF COUNSEL
Street Address: 875 NORTH RANDOLPH STREET
City: ARLINGTON
State: VA Zip: 22203-1995
Phone Number: 703-696-4008
Fax Number: 703-696-6909
Email Address: CAROL.PETROSKY@NAVY.MIL

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 1.21(h) & 3.41) $

☐ Authorized to be charged to deposit account
☐ Enclosed
☒ None required (government interest not affecting title)

8. Payment Information

Deposit Account Number

Authorized User Name

9. Signature:

(b) (6) [redacted]

07/19/2011
Date

CAROL PETROSKY
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 2

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

License to the United States Government

Sign and Fax this to (301) 480-0272

Invention Title: Optimized Vertical Power DMOSFETS in Silicon Carbide

Inventor(s): Asmita Saha, James A. Cooper

U.S. Filing/Issue Date: 1/23/06

Patent or Application Serial No.: 11/338,007

Grant/Contract Number(s): N00014-02-1-0628

Foreign Applications filed/intended in (countries): _____

The invention identified above is a Subject Invention under **35 U.S.C. 200, et seq.**, and the Standard Patent Rights clause at **37 CFR 401.14, FAR 52.227-11** or **FAR 52.227-12** (if applicable) which are included among the terms of the above identified grant or contract award from the United State Government. This document is confirmatory of:

1. The nonexclusive, nontransferable, irrevocable, paid-up license to practice or have practiced for or on behalf of the United States the invention described in any patent application and in any and all divisions, continuations, and continuations in part, and in any and all patents and re-issues granted thereon throughout the world; and
2. All other rights acquired by the Government by reason of the above identified grant/contract award and the laws and regulations that are applicable to the award.

The Government is hereby granted an irrevocable power to inspect and make copies of the above-identified patent application.

Signed this 7th day of July , 20 06 .

By Joseph B. Hornett (b) (6)
(Name of Grantee/Contractor Official)

Title Senior Vice President and Treasurer

For PURDUE UNIVERSITY
(Grantee/Contractor Organization)

At Office of Technology Commercialization Purdue Research Foundation 3000 Kent Avenue WEST

LAFAYETTE, IN 47906 US
(Business Address)

REQ708021226 WNR-01-11-054-2-009-01-004

ARR1-554641137

Transfer#: W298-07-0001 **Box:1 CC:00**

Asset#: AAC1-24157692 **Whole Container: N**

C/F: N00014-99-1-0310 - MIT **Created:** 8/2/2012

	General Reference	Temporary Loan of Records
Standard	Standard (billed)	N/A

To: TONYA KILGORE
OFFICE OF NAVAL RESEARCH875 NORTH RANDOLPH STREET , CODE 42, RM 619
ARLINGTON, VA, 22203-1995
P : (703) 696-4623 F : (703) 696-4097

(b) (6)

8/8/12

BARNES & THORNBURG LLP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Customer No.	23643
Group:	2811
Confirmation No.:	4085
Application No.:	11/338,007
Invention:	HIGH-VOLTAGE POWER SEMICONDUCTOR DEVICE
Inventor:	James A. Cooper et al.
Filed:	January 23, 2006
Attorney Docket:	3220-79132
Examiner:	Unknown

Certificate Under 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

on 4/10/06

(b) (6)

Karla Mays
(Printed Name)

PRELIMINARY AMENDMENT UNDER 37 C. F. R. §1.115(a)

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sirs:

Preliminary to the examination of the above-identified national patent application, claiming priority to U.S. Provisional Patent Application No. 60/646,152, Applicants request entry of the amendment to the specification indicated below.

IN THE SPECIFICATION:

Under 37 C.F.R. § 1.121(b) please insert the following after the Title on page 1:

This invention was made with support from DARPA/MTO Grant No. N00014-02-1-0628; the government may have certain rights in this invention.

REMARKS

Applicants do not believe that any fees are due with this Preliminary Amendment; however, the Commissioner is authorized to charge any fees that may be due with this amendment to the deposit account of Barnes & Thornburg account No. (b) (6) with reference to our matter No. 3220-79132.

Respectfully submitted,

BARNES & THORNBURG

(b) (6)

Bradford G. Addison
Registration No. 41,486
Attorney for Applicants

BGA/gmk
Indianapolis, IN
(317) 231-7253

UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

JULY 17, 2006

PTAS

103251548A

CAROL PETROSKY
OFFICE OF NAVAL RESEARCH
OFFICE OF COUNSEL
875 NORTH RANDOLPH STREET
ARLINGTON, VA 22203-1995

UNITED STATES PATENT AND TRADEMARK OFFICE
NOTICE OF RECORDATION OF ASSIGNMENT DOCUMENT

THE ENCLOSED DOCUMENT HAS BEEN RECORDED BY THE ASSIGNMENT DIVISION OF THE U.S. PATENT AND TRADEMARK OFFICE. A COMPLETE MICROFILM COPY IS AVAILABLE AT THE ASSIGNMENT SEARCH ROOM ON THE REEL AND FRAME NUMBER REFERENCED BELOW.

PLEASE REVIEW ALL INFORMATION CONTAINED ON THIS NOTICE. THE INFORMATION CONTAINED ON THIS RECORDATION NOTICE REFLECTS THE DATA PRESENT IN THE PATENT AND TRADEMARK ASSIGNMENT SYSTEM. IF YOU SHOULD FIND ANY ERRORS OR HAVE QUESTIONS CONCERNING THIS NOTICE, YOU MAY CONTACT THE EMPLOYEE WHOSE NAME APPEARS ON THIS NOTICE AT 571-272-3350. PLEASE SEND REQUEST FOR CORRECTION TO: U.S. PATENT AND TRADEMARK OFFICE, MAIL STOP: ASSIGNMENT SERVICES BRANCH, P.O. BOX 1450, ALEXANDRIA, VA 22313.

RECORDATION DATE: 05/22/2006
REEL/FRAME: 017944/0901
NUMBER OF PAGES: 2

BRIEF: CONFIRMATORY LICENSE (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
PURDUE UNIVERSITY
DOC DATE: 03/24/2006

ASSIGNEE:
NAVY, SECRETARY OF THE, UNITED
STATES OF AMERICA
875 NORTH RANDOLPH STREET
OFFICE OF NAVAL RESEARCH
ARLINGTON, VIRGINIA 22203-1995

SERIAL NUMBER: 11338043
FILING DATE: 01/23/2006
PATENT NUMBER.
ISSUE DATE:
TITLE: METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE

ANTIONE ROYALL, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

D 8

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

06-06-2006

103251548

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

5/22/06

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies)

PURDUE UNIVERSITY

Additional name(s) of conveying party(ies) attached? ☐ Yes ☑ No

MAY 22 2006 PATENT & TRADEMARK OFFICE

2. Name and address of receiving party(ies)

Name: NAVY, SECRETARY OF THE,UNITED STATES OF

Internal Address: AMERICA

OFFICE OF NAVAL RESEARCH

Street Address: 875 NORTH RANDOLPH STREET

City: ARLINGTON

State: VA

Country: USA Zip: 22203-1995

Additional name(s) & address(es) attached? ☐ Yes ☑ No

3. Nature of conveyance/Execution Date(s):

Execution Date(s) 03/24/06

☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☑ Executive Order 9424, Confirmatory License
☐ Other

4. Application or patent number(s):

☐ This document is being filed together with a new application.

A. Patent Application No.(s)

11/338,043

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☑ No

5. Name and address to whom correspondence concerning document should be mailed:

Name: CAROL PETROSKY

Internal Address: OFFICE OF NAVAL RESEARCH

OFFICE OF COUNSEL

Street Address: 875 NORTH RANDOLPH STREET

City: ARLINGTON

State: VA Zip: 22203-1995

Phone Number: 703-696-4008

Fax Number: 703-696-6909

Email Address: PETROSC@ONR.NAVY.MIL

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 1.21(h) & 3.41) $

☐ Authorized to be charged by credit card
☐ Authorized to be charged to deposit account
☐ Enclosed
☐ None required (government interest not affecting title)

8. Payment Information

a. Credit Card Last 4 Numbers
Expiration Date

b. Deposit Account Number CUSTOMER NUMBER

Authorized User Name 26852

9. Signature:

(b) (6)

5/17/06
Date

JAMES BECHTEL
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents:

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

License to the United States Government

Sign and Fax this to (301) 480-0272

Invention Title: High-Voltage N-Channel Insulated Gate Bipolar Tansistor (IGBT) in Silicon Carbide

Inventor(s): Xiaokun Wang, James A. Cooper

U.S. Filing/Issue Date: 1/23/06

Patent or Application Serial No.: 11/338,043

Grant/Contract Number(s): N00014-02-1-0628

Foreign Applications filed/intended in (countries): _____

The invention identified above is a Subject Invention under **35 U.S.C. 200, et seq.**, and the Standard Patent Rights clause at **37 CFR 401.14, FAR 52.227-11** or **FAR 52.227-12** (if applicable) which are included among the terms of the above identified grant or contract award from the United State Government. This document is confirmatory of:

1. The nonexclusive, nontransferable, irrevocable, paid-up license to practice or have practiced for or on behalf of the United States the invention described in any patent application and in any and all divisions, continuations, and continuations in part, and in any and all patents and re-issues granted thereon throughout the world; and
2. All other rights acquired by the Government by reason of the above identified grant/contract award and the laws and regulations that are applicable to the award.

The Government is hereby granted an irrevocable power to inspect and make copies of the above-identified patent application.

Signed this 24th day of March, 20 06

By Joseph B. Hornett [redacted]
(Name of Grantee/Contractor Official)

Title Senior Vice President and Treasurer

For PURDUE UNIVERSITY
(Grantee/Contractor Organization)

At Office of Technology Commercialization Purdue Research Foundation 3000 Kent Avenue WEST LAFAYETTE, IN 47906 US
(Business Address)

Petrosky, Carol

From: edison@od.nih.gov
Sent: Friday, July 07, 2006 8:47 AM
To: Petrosky, Carol
Subject: iEdison Notification of Patent Confirmatory License Modification

The confirmatory license for the following invention report was modified by Sally Ross on 7/7/06 8:46 AM in the Interagency Edison system.

Invention Report Number: 1481401-05-0026
Patent Docket Number: 64281.00.US

Should you wish to verify the change, you may go to the Interagency Edison system, log in, and view the record for this invention/patent.

Should you have any questions or issues relative to this action, please contact iEdison User Support at edison@od.nih.gov, (301) 435-1986, or toll-free (866) 504-9552.

C64281

License to the United States Government

Sign and Fax this to (301) 480-0272

Invention Title: Optimized Vertical Power DMOSFETS in Silicon Carbide

Inventor(s): Asmita Saha, James A. Cooper

U.S. Filing/Issue Date: 1/23/06

Patent or Application Serial No.: 11/338,007

Grant/Contract Number(s): N00014-02-1-0628

Foreign Applications filed/intended in (countries):

The invention identified above is a Subject Invention under **35 U.S.C. 200, et seq.**, and the Standard Patent Rights clause at **37 CFR 401.14, FAR 52.227-11** or **FAR 52.227-12** (if applicable) which are included among the terms of the above identified grant or contract award from the United State Government. This document is confirmatory of:

1. The nonexclusive, nontransferable, irrevocable, paid-up license to practice or have practiced for or on behalf of the United States the invention described in any patent application and in any and all divisions, continuations, and continuations in part, and in any and all patents and re-issues granted thereon throughout the world; and
2. All other rights acquired by the Government by reason of the above identified grant/contract award and the laws and regulations that are applicable to the award.

The Government is hereby granted an irrevocable power to inspect and make copies of the above-identified patent application.

Signed this 7th day of July 20 06

By Joseph B. Hornett
(Name of Grantee/Contractor Official)

(b) (6)
(Signature)

Title Senior Vice President and Treasurer

For PURDUE UNIVERSITY
(Grantee/Contractor Organization)

At Office of Technology Commercialization Purdue Research Foundation 3000 Kent Avenue WEST LAFAYETTE, IN 47906 US
(Business Address)

Form PTO-1595 (Rev. 07/05)
OMB No. 0651-0027 (exp. 6/30/2008)

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

RECORDATION FORM COVER SHEET
PATENTS ONLY

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies)

PURDUE UNIVERSITY

Additional name(s) of conveying party(ies) attached? ☐ Yes ☑ No

2. Name and address of receiving party(ies)

Name: NAVY, SECRETARY OF THE,UNITED STATES OF
Internal Address: AMERICA
OFFICE OF NAVAL RESEARCH
Street Address: 875 NORTH RANDOLPH STREET
City: ARLINGTON
State: VA
Country: USA Zip: 22203-1995

Additional name(s) & address(es) attached? ☐ Yes ☑ No

3. Nature of conveyance/Execution Date(s):

Execution Date(s) 03/24/06

☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☑ Executive Order 9424, Confirmatory License
☐ Other

4. Application or patent number(s):

☐ This document is being filed together with a new application.

A. Patent Application No.(s)

11/338,043

B. Patent No.(s)

Additional numbers attached? ☐ Yes ☑ No

5. Name and address to whom correspondence concerning document should be mailed:

Name: CAROL PETROSKY
Internal Address: OFFICE OF NAVAL RESEARCH
OFFICE OF COUNSEL
Street Address: 875 NORTH RANDOLPH STREET
City: ARLINGTON
State: VA Zip: 22203-1995
Phone Number: 703-696-4008
Fax Number: 703-696-6909
Email Address: PETROSC@ONR.NAVY.MIL

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 1.21(h) & 3.41) $

☐ Authorized to be charged by credit card
☐ Authorized to be charged to deposit account
☐ Enclosed
☐ None required (government interest not affecting title)

8. Payment Information

a. Credit Card Last 4 Numbers
Expiration Date

b. Deposit Account Number CUSTOMER NUMBER

Authorized User Name 26852

9. Signature:

(b) (6)

5/17/06
Date

JAMES BECHTEL
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents:

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

Petrosky, Carol

From: edison@od.nih.gov
Sent: Friday, June 16, 2006 10:38 AM
To: Petrosky, Carol
Subject: iEdison Notification of Government Support Clause Modification

License already received

The government support clause associated with the following invention report/patent report was modified by Sally Ross on 6/16/06 10:37 AM in the Interagency Edison system.

Invention Report Number: 1481401-05-0025
Patent Docket Number: 64280.00.US

Should you wish to verify the change, you may go to the Interagency Edison system, log in, and view the record for this invention.

Should you have any questions or issues relative to this action, please contact iEdison User Support at edison@od.nih.gov, (301) 435-1986, or toll-free (866) 504-9552.

64280

02-1-6628

BARNES & THORNBURG LLP

Bradford G. Addison
(317) 231-7253
Email: bradford.addison@btlaw.com

11 South Meridian Street
Indianapolis, IN 46204-3535
(317) 236-1313
Fax (317) 231-7433

www.btlaw.com

April 19, 2006

VIA E-MAIL

Ms. Simran Trana
Purdue Research Foundation
Office of Technology Communication
3000 Kent Avenue
West Lafayette, IN 47906

Re: U.S. Utility Patent Application Serial No. 11/338,043
Title: METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE
Your Reference: 64280.00.US
Our Matter: 3220-79131

Dear Simran:

Please find enclosed a copy of a Preliminary Amendment and related document that were filed in the U.S. Patent and Trademark Office on April 10, 2006 in the above-referenced matter. As always, if you should have any questions, please do not hesitate to contact me.

Very truly yours,

BARNES & THORNBURG LLP

(b) (6)

Bradford G. Addison

BGA/GMK/kim
Enclosures

Mailed:	April 10, 2006
Applicant:	James A. Cooper et al.
Invention:	**METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE**
Serial No:	11/338,043
Filed:	January 23, 2006
Docket:	3220-79131

X Preliminary Amendment Under 37 C.F.R. §1.115(a)

The stamp of the Patent Office hereon shows receipt of the indicated papers.

BGAGMK/kim

BARNES & THORNBURG LLP

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Customer No.	23643
Group:	2812
Confirmation No.:	5161
Application No.:	11/338,043
Invention:	METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE
Inventor:	James A. Cooper et al.
Filed:	January 23, 2006
Attorney Docket:	3220-79131
Examiner:	Unknown

Certificate Under 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

on 4/10/06

(b) (6) [redacted]
(Signature)

Karla Mays
(Printed Name)

PRELIMINARY AMENDMENT UNDER 37 C. F. R. §1.115(a)

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sirs:

Preliminary to the examination of the above-identified national patent application, claiming priority to U.S. Provisional Patent Application No. 60/646,151, Applicants request entry of the amendment to the specification indicated below.

IN THE SPECIFICATION:

Under 37 C.F.R. § 1.121(b) please insert the following after the Title on page 1:

This invention was made with support from DARPA/MTO Grant No. N00014-02-1-0628; the government may have certain rights in this invention.

REMARKS

Applicants do not believe that any fees are due with this Preliminary Amendment; however, the Commissioner is authorized to charge any fees that may be due with this amendment to the deposit account of Barnes & Thornburg account No. (b) (6) with reference to our matter No. 3220-79131.

Respectfully submitted,

BARNES & THORNBURG

(b) (6)

Bradford G. Addison
Registration No. 41,486
Attorney for Applicants

BGA/gmk
Indianapolis, IN
(317) 231-7253

Petrosky, Carol

From: edison@od.nih.gov
Sent: Tuesday, April 25, 2006 1:02 PM
To: Petrosky, Carol
Subject: iEdison Notification of Patent Confirmatory License Modification

The confirmatory license for the following invention report was modified by Sally Ross on 4/25/06 1:01 PM in the Interagency Edison system.

Invention Report Number: 1481401-05-0025
Patent Docket Number: 64280.00.US

Should you wish to verify the change, you may go to the Interagency Edison system, log in, and view the record for this invention/patent.

Should you have any questions or issues relative to this action, please contact iEdison User Support at edison@od.nih.gov, (301) 435-1986, or toll-free (866) 504-9552.

64280

027-0622

License to the United States Government

Sign and Fax this to (301) 480-0272

Invention Title: High-Voltage N-Channel Insulated Gate Bipolar Tansistor (IGBT) in Silicon Carbide

Inventor(s): Xiaokun Wang, James A. Cooper

U.S. Filing/Issue Date: 1/23/06

Patent or Application Serial No.: 11/338,043

Grant/Contract Number(s): N00014-02-1-0628

Foreign Applications filed/intended in (countries): _____

The invention identified above is a Subject Invention under **35 U.S.C. 200, et seq.**, and the Standard Patent Rights clause at **37 CFR 401.14, FAR 52.227-11** or **FAR 52.227-12** (if applicable) which are included among the terms of the above identified grant or contract award from the United State Government. This document is confirmatory of:

1. The nonexclusive, nontransferable, irrevocable, paid-up license to practice or have practiced for or on behalf of the United States the invention described in any patent application and in any and all divisions, continuations, and continuations in part, and in any and all patents and re-issues granted thereon throughout the world; and
2. All other rights acquired by the Government by reason of the above identified grant/contract award and the laws and regulations that are applicable to the award.

The Government is hereby granted an irrevocable power to inspect and make copies of the above-identified patent application.

Signed this 24th day of March, 20 06.

By Joseph B. Hornett
(Name of Grantee/Contractor Official)

(b) (6)
(Signature)

Title Senior Vice President and Treasurer

For PURDUE UNIVERSITY
(Grantee/Contractor Organization)

At Office of Technology Commercialization Purdue Research Foundation 3000 Kent Avenue WEST LAFAYETTE, IN 47906 US
(Business Address)

Petrosky, Carol

From: edison@od.nih.gov
Sent: Tuesday, March 21, 2006 10:06 AM
To: Petrosky, Carol
Subject: iEdison Not Elect Title Notification

PURDUE UNIVERSITY has chosen not to elect title for the following invention report submitted on 03/21/2006 10:06 am in the Interagency Edison system.

Invention Report Number: 1481401-05-0024

Should you have any questions or issues relative to this action, please contact iEdison User Support at edison@od.nih.gov, (301) 435-1986, or toll-free (866) 504-9552.

021-0628

Petrosky, Carol

From: edison@od.nih.gov
Sent: Tuesday, October 18, 2005 3:58 PM
To: Petrosky, Carol
Subject: iEdison Invention Disclosure Modified Notification

The invention disclosure document associated with the following invention report was modified by Molly Byers on 10/18/05 3:58 PM in the Interagency Edison system.

Invention Report Number: 1481401-05-0026

Should you wish to verify the change, you may go to the Interagency Edison system, log in, and view the record for this invention.

Petrosky, Carol

From: edison@od.nih.gov
Sent: Tuesday, October 18, 2005 3:46 PM
To: Petrosky, Carol
Subject: iEdison Invention Disclosure Modified Notification

The invention disclosure document associated with the following invention report was modified by Molly Byers on 10/18/05 3:46 PM in the Interagency Edison system.

Invention Report Number: 1481401-05-0025

Should you wish to verify the change, you may go to the Interagency Edison system, log in, and view the record for this invention.

Petrosky, Carol

From: edison@od.nih.gov
Sent: Tuesday, October 18, 2005 3:26 PM
To: Petrosky, Carol
Subject: iEdison Invention Disclosure Modified Notification

The invention disclosure document associated with the following invention report was modified by Molly Byers on 10/18/05 3:26 PM in the Interagency Edison system.

Invention Report Number: 1481401 05 0024

Should you wish to verify the change, you may go to the Interagency Edison system, log in, and view the record for this invention.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

SEPTEMBER 08, 2010

PTAS

203606157A

CAROL PETROSKY.
OFFICE OF NAVAL RESEARCH
OFFICE OF COUNSEL
875 NORTH RANDOLPH STREET
ARLINGTON, VA 22203-1995

UNITED STATES PATENT AND TRADEMARK OFFICE
NOTICE OF RECORDATION OF ASSIGNMENT DOCUMENT

THE ENCLOSED DOCUMENT HAS BEEN RECORDED BY THE ASSIGNMENT DIVISION OF THE U.S. PATENT AND TRADEMARK OFFICE, A COMPLETE MICROFILM COPY IS AVAILABLE AT THE ASSIGNMENT SEARCH ROOM ON THE REEL AND FRAME NUMBER REFERENCED BELOW.

PLEASE REVIEW ALL INFORMATION CONTAINED ON THIS NOTICE. THE INFORMATION CONTAINED ON THIS RECORDATION NOTICE REFLECTS THE DATA PRESENT IN THE PATENT AND TRADEMARK ASSIGNMENT SYSTEM. IF YOU SHOULD FIND ANY ERRORS OR HAVE QUESTIONS CONCERNING THIS NOTICE, YOU MAY CONTACT THE EMPLOYEE WHOSE NAME APPEARS ON THIS NOTICE AT 571-272-3350. PLEASE SEND REQUEST FOR CORRECTION TO: U.S. PATENT AND TRADEMARK OFFICE, MAIL STOP: ASSIGNMENT SERVICES BRANCH, P.O. BOX 1450, ALEXANDRIA, VA 22313.

RECORDATION DATE: 09/02/2010
REEL/FRAME: 024943/0094
NUMBER OF PAGES: 2

BRIEF: CONFIRMATORY LICENSE (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
PURDUE UNIVERSITY
DOC DATE: 02/22/2010

ASSIGNEE:
NAVY, SECRETRY OF THE UNITED
STATES OF AMERICA
875 NORTH RANDOLPH STREET
OFFICE OF NAVAL RESEARCH
ARLINGTON, VIRGINIA 22203-1995

SERIAL NUMBER: 12429176
FILING DATE: 04/23/2009
PATENT NUMBER:
ISSUE DATE:
TITLE: SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACTS AND METHOD FOR MAKING THE SAME

KIMBERLY WHITE, EXAMINER
ASSIGNMENT SERVICES BRANCH
PUBLIC RECORDS DIVISION

9/2/10

Form PTO-1595 (Rev. 03-09)
OMB No. 0651-0027 (exp. 03/31/2009)

09-02-2010

103606157

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

:T

To the Director of the U.S. Patent an.

ocuments or the new address(es) below.

1. Name of conveying party(ies)

PURDUE UNIVERSITY

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)

Name: NAVY, SECRETRY OF THE UNITED STATES

Internal Address: OF AMERICA

OFFICE OF NAVAL RESEARCH

Street Address: 875 NORTH RANDOLPH STREET

City: ARLINGTON

State: VA

Country: USA Zip: 22203-1995

Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance/Execution Date(s):

Execution Date(s) 02/22/2010

☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☒ Executive Order 9424, Confirmatory License
☐ Other

4. Application or patent number(s):

☐ This document is being filed together with a new application.

A. Patent Application No.(s)

12/429,176

B. Patent No.(s)

Assignment Recordation Branch
Received
SEP 2 2010
5th Floor
Public Records Division

Additional numbers attached? ☐ Yes ☒ No

5. Name and address to whom correspondence concerning document should be mailed:

Name: CAROL PETROSKY

Internal Address: OFFICE OF NAVAL RESEARCH

OFFICE OF COUNSEL

Street Address: 875 NORTH RANDOLPH STREET

City: ARLINGTON

State: VA Zip: 22203-1995

Phone Number: 703-696-4008

Fax Number: 703-696-6909

Email Address: CAROL.PETROSKY@NAVY.MIL

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 1.21(h) & 3.41) $

☐ Authorized to be charged to deposit account
☐ Enclosed
☒ None required (government interest not affecting title)

8. Payment Information

Deposit Account Number

Authorized User Name

9. Signature:

(b) (6)

Signature

08/12/2010
Date

CAROL PETROSKY
Name of Person Signing

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A. Patent Application No.(s)

12/429,176

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Name: CAROL PETROSKY
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Phone Number: 703-696-4008
Fax Number: 703-696-6909
Email Address: CAROL.PETROSKY@NAVY.MIL

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Invention Title: SiC Power DMOSFETs with Self-Aligned Source Contacts

Inventor(s): Asmita Saha, James A. Cooper, Jr.

U.S. Filing/Issue Date: 4/23/2009

Patent or Application Serial No.: 12/429,176

Grant/Contract Number(s): N00014-05-1-0437

Foreign Applications filed/intended in (countries):

The invention identified above is a Subject Invention under **35 U.S.C. 200, et seq.**, and the Standard Patent Rights clause at **37 CFR 401.14, FAR 52.227-11** or **FAR 52.227-12** (if applicable) which are included among the terms of the above identified grant or contract award from the United State Government. This document is confirmatory of:

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By Joseph B Hornett [redacted]
(Name of Grantee/Contractor Official)

Title Senior Vice President and Treasurer

For PURDUE UNIVERSITY
(Grantee/Contractor Organization)

At Office of Technology Commercialization Purdue Research Foundation 1281 Win Hentschel Blvd. West Lafayette, IN 47906 US
(Business Address)

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SERIAL NUMBER: 12429176

FILING DATE: 04/23/2009

PATENT NUMBER:

ISSUE DATE:

TITLE: SIC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACTS AND METHOD FOR MAKING THE SAME

051-0437

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~~0423~~ 97

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☒ Executive Order 9424, Confirmatory License
☐ Other

4. Application or patent number(s):

☐ This document is being filed together with a new application.

A. Patent Application No.(s)

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B. Patent No.(s)

Additional numbers attached? ☐ Yes ☒ No

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Petrosky, Carol

From: edison@od.nih.gov
Sent: Monday, February 22, 2010 3:34 PM
To: Petrosky, Carol
Subject: iEdison Notification of Patent Confirmatory License Modification

The confirmatory license for the following invention report was modified by Melissa Franks on 2/22/10 3:33 PM in the Interagency Edison system.

Invention Report Number: 1481401-08-0027 Patent Docket Number: 65034.00.US

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Invention Title: SiC Power DMOSFETs with Self-Aligned Source Contacts

Inventor(s): Asmita Saha, James A. Cooper, Jr.

U.S. Filing/Issue Date: 4/23/2009

Patent or Application Serial No.: 12/429,176

Grant/Contract Number(s): N00014-05-1-0437

Foreign Applications filed/intended in (countries):

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Signed this 22nd day of February ,20 10

By Joseph B Hornett
(Name of Grantee/Contractor Official)

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(Signature)

Title Senior Vice President and Treasurer

For PURDUE UNIVERSITY
(Grantee/Contractor Organization)

At Office of Technology Commercialization Purdue Research Foundation 1281 Win Hentschel Blvd. West Lafayette, IN 47906 US
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April 27, 2009

Hilton A. Turner, Jr.
Innovation Strategy Manager
Purdue Research Foundation
1281 Win Hentschel Boulevard
West Lafayette, IN 47906-4182

Re: U.S. Patent Application No. 12/429,176
Filed April 23, 2009
SiC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACTS AND METHOD FOR MAKING THE SAME
Inventors: James A. Cooper et al.
Purdue Ref.: 65034.00.US
Our Ref.: 13054-285A

Dear Hilton:

We have now completed and filed a regular utility patent application as authorized for the above-identified invention. A copy of the application as filed is enclosed for your records. The accompanying Declaration is not for signature; we will forward a fresh Declaration for signature in the near future.

We anticipate receiving the official filing receipt from the Patent Office within the next 30-60 days, and we will forward it to you upon receipt. In the meantime, please feel free to give me a call if you have any questions.

Note that inventors have a duty to disclose material prior art, including prior products, patents, publications, etc. If you know of any prior art that may be pertinent, please bring it to my attention so that I can include it in an Information Disclosure Statement along with some prior art of which I am already aware.

Our thanks to Jim Cooper for his assistance during the preparation of this application.

Best regards.

Sincerely,

(b) (6)

William F. Bahret

WFB/jce
Enclosures
cc: James A. Cooper (w/ encls.)

SiC POWER DMOSFET WITH SELF-ALIGNED SOURCE CONTACTS AND METHOD FOR MAKING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit of U.S. Provisional Patent Application Serial No. 61/047,274, filed April 23, 2008, which application is hereby incorporated by reference.

GOVERNMENT RIGHTS

This invention was made with government support under Contract/Grant No. W56HZV-06-C-0228 awarded by the U. S. Army TACOM LCMC. The government has certain rights in the invention.

BACKGROUND OF THE INVENTION

This invention relates generally to semiconductor field effect transistors, and more particularly to field effect transistors having self-aligned source contacts.

The metal oxide semiconductor field effect transistor (MOSFET) is a device used to amplify or switch electronic signals. Power MOSFETs are well known for their ability to carry large currents in the on-state while withstanding large breakdown voltages in the off-state. In such devices, current flow between source and drain regions in a semiconductor substrate is controlled by a voltage applied to a gate electrode that is separated from the semiconductor surface by an insulator, typically silicon dioxide. In an n-type enhancement MOSFET, for example, a positive bias on the gate causes a surface inversion layer – or channel – to form in a p-type region under the gate oxide and thereby creates a conductive path between source and drain. The application of a positive drain voltage then produces current flow between drain and source. Lateral and vertical power MOSFET structures in silicon have been explored over the years, the former type having the drain, gate and source terminals on the same surface of the silicon wafer, the latter type having the source and drain

on opposite surfaces of the wafer. Several different types of vertical power MOSFETs have been proposed, including the double-diffused MOSFET (DMOSFET) and the trench-gate or UMOSFET. These and other power MOSFETs are described in a textbook by B. Jayant Baliga entitled Power Semiconductor Devices, PWS Publishing Co. (1996), the disclosure of, which is hereby incorporated herein by reference.

Although silicon has been the material of choice for many semiconductor applications, its fundamental electronic structure and characteristics prevent its utilization beyond certain parameters. Thus, interest in power MOSFET devices has turned from silicon to other materials, including silicon carbide. SiC power switching devices have significant advantages over silicon devices, including faster switching speed, lower specific on-resistance and thus lower power losses. SiC has a breakdown electric field that is an order of magnitude higher than that of silicon, which allows for a thinner drift region and thus a lower drift region resistance.

In power DMOSFETs, an important performance parameter is the specific on-resistance ($R_{ON,SP}$), which is defined as the product of the resistance when the device is in the "on", or highly conducting, state (low V_{DS}), times the area of the device (units are Ω-cm^2 or mΩ-cm^2). Thus it is important to minimize both the resistance and the area of the device. For DMOSFETs in the blocking voltage regime of below about 600-1800V, a significant component of the total resistance is the resistance of the source contacts. Larger-area source contacts obviously have lower resistance, but increasing the contact area increases the total area of the device, and hence $R_{ON,SP}$. It is important to find ways to reduce the source contact resistance without increasing the area of the device.

In a conventional DMOSFET, the source contact is defined by photolithography, and the source contact must be separated from the edge of the gate by sufficient distance so that the source contact and gate cannot touch even under worst-case misalignment of the source contact mask. In addition, the actual functional area of the source contact is determined by the overlap of the source contact metal and the N+ implant that forms the source region in the semiconductor. Since the N+ implant is defined by a separate mask, relative misalignment of the source contact mask and the N+ implant mask can reduce the functional area of the source contact, thereby increasing source resistance and degrading performance.

It is desired to produce DMOSFETs and related devices wherein misalignments of source contact and gate are reduced or eliminated.

5

SUMMARY OF THE INVENTION

The present invention provides high voltage power MOSFETs, with self aligned source contacts and a method for making the same.

An intermediate product in the fabrication of a MOSFET, including a silicon carbide wafer having a substrate and a drift layer on said substrate, said drift layer having a plurality of source regions formed adjacent an upper surface thereof; a first oxide layer on said upper surface of said drift layer; a plurality of polysilicon gates above said first oxide layer, said plurality of polysilicon gates including a first gate adjacent a first of said source regions; an oxide layer over said first source region of greater thickness than said first oxide layer; and, an oxide layer over said first gate of substantially greater thickness than said oxide layer over said first source region.

These and other aspects and advantages of the present invention will become more apparent upon reading the following detailed description of preferred embodiments in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a side, cross-sectional view of one cell region 10 of a perfectly aligned, conventional DMOSFET 11.

FIG. 2 is a side, cross-sectional view of the one cell region 10 of FIG. 1 in a worst-case mask misaligned fabrication.

FIG. 3 is a side, cross-sectional view of one cell region 20 of a DMOSFET 21 in accordance with the present invention.

FIG. 4 is a side, cross-sectional view of the cell region 20 of FIG. 3 and shown shifted one half cell width laterally from the view of FIG. 3.

FIGS. 5-8 are side, cross-sectional views of one cell region of an intermediate semiconductor product 58 showing various intermediate stages of fabrication of the DMOSFET 21 of Fig. 3.

FIG. 9 is a layout view of a 10 A DMOSFET formed in accordance with the present invention

FIG. 10 is a wafer photograph showing gate and source fingers of the DMOSFET OF FIG. 9 in more detail.

Description of Preferred Embodiments

For the purpose of promoting an understanding of the principles of the invention, reference will now be made to the embodiments illustrated in the drawings and specific language will be used to describe the same. It will nevertheless be understood that no limitation of the scope of the invention is thereby intended, and that alterations and further modifications in the illustrated device and further applications of the principles of the invention as illustrated therein are contemplated as would normally occur to one skilled in the art to which the invention relates. As shown in the Figures, the sizes of some layers or regions are exaggerated to better illustrate the general structures of the present invention, and actual sizes – often with thicknesses of 50 nm – are either specified or are understood by persons of skill in the art to be other than that shown in the Figures.

It is desired in power DMOSFETs to have a low specific on-resistance ($R_{ON,SP}$), which is defined as the product of the resistance when the device is in the "on", or highly conducting, state (low V_{DS}), times the area of the device (units are Ω-cm^2 or mΩ-cm^2). It is therefore important to minimize both the resistance and the area of the device. For DMOSFETs with blocking voltage below about 1800V, a significant component of the total resistance is the resistance of the source contacts. While larger-area source contacts obviously have lower resistance, they conversely increase the total area of the device, and hence $R_{ON,SP}$.

Referring to FIG. 1, there is shown one cell region 10 of a perfectly aligned, conventional DMOSFET 11. In DMOSFET 11, the source contact 13 is defined by photolithography, and source contact 13 must be separated from the edge of the gate 14 by sufficient distance **X** so that source contact 13 and gate 14 cannot touch even under worst-case misalignment of the source contact mask. In addition, the actual functional area of the source contact is determined by the overlap **A** of the source contact metal 13 and the N+ implant 15 that forms the source region in the semiconductor. Since the N+ implant 15 is defined by a separate mask, relative misalignment of the source contact mask and the N+ implant mask can reduce the functional area of the source contact, thereby increasing source resistance and degrading performance. A worst-case mask misaligned is shown in FIG. 2 where the Ni metal for the source contact 13′ has been misaligned to the right and the P+

implant 17 for the P+ base contact 18 has been misaligned to the left. The resulting overlap **B** of Ni metal and N+ implant has been reduced almost to zero, resulting in a very large contact resistance for this part of the device. Another drawback of this approach is the alignment tolerance (spacing **X**) that must be built into the MOSFET design to ensure that the source metal 13 never comes into contact with gate 14 under worst-case misalignment. That is, if the MOSFET design parameters require that source metal 13 never get closer to gate 14 than spacing **Y**, even under a worst-case mask misalignment (as shown in FIG. 2), then the target mask alignment must be performed with a spacing **X**. The necessary additional spacing (which is the difference between **X** and **Y**) unduly increases the area of the cell, and thus increases $R_{ON,SP}$. Both these problems – increased contact resistance at reduced area overlap **B** from mask misalignment and increased cell width to ensure adequate spacing **Y** - are eliminated in the present invention by negating the opportunity for misalignment of source contact metal and gate.

Referring to FIG. 3, there is shown one cell region 20 of a double-diffused, power metal-oxide-semiconductor field effect transistor (DMOSFET) 21 in accordance with the present invention. While this and other embodiments presented herein are directed to power DMOSFETs and method for making the same, the present invention is believed to be applicable in varying degrees to other MOSFET designs or similar semiconductor geometry having a source and a gate where it is desirable to place the source and gate as close together as possible and/or to minimize or reduce mask misalignment errors relating to positionment of the gate and source. Such other MOSFETs contemplated by the present invention include, but are not limited to, other vertical MOSFETS, e.g., VMOSFETs and UMOSFETs, as well as lateral DMOSFETs.

DMOSFET 21 includes a substrate 23 and a number of semiconductor layers and implants formed on or in the substrate 23 up through top surface 28, collectively referred to as the substrate body 22. The fabrication of substrate body 22, and variations thereof, can be accomplished in a variety of ways well known in the art and not substantially discussed herein. Substrate 23 and the layers and implants are formed from silicon-carbide and doped with N-type or P-type impurities as shown in FIG. 3 and described herein. In addition to the embodiments described, alternative embodiments are contemplated wherein the compositions

and configurations of the layers and implants, of the impurity concentrations, and of the method and timing of impurity doping and implant creation differs from that described herein and is in any manner suitable for the intended MOSFET task. Substrate 23 is heavily doped with N-type impurities to an "N+" concentration. Formed atop substrate 23 is drift layer 24, which is lightly doped to an "N-" concentration. Atop drift layer 24 is formed a current spreading epilayer (CSL) 25, which is more heavily doped than drift layer 24, but not as heavily doped as substrate 23. Alternative embodiments are contemplated wherein there is no separately formed CSL layer, and the drift layer 24 extends all the way to the top SiC surface 28. Formed in the top of the current spreading layer 25 is a P well 29. The conductivity types may alternatively be the opposite of those described above. That is, both n-channel and p-channel devices are contemplated as part of the present invention.

It should be understood that the semiconductor device (MOSFET 21) of FIG. 3 may be a single "transistor cell" and that a completely fabricated transistor device may include any number of such semiconductor devices or cells. As such, the present description relating to cell region 20 is with the understanding that the description is applicable to all semiconductor devices that form a larger, fabricated transistor device. For example, the fabricated transistor device may include any number of doped semiconductor wells 29 depending on the number of semiconductor cell regions 20 included therein. In addition, the present embodiment is directed to an interdigitated finger array (as shown in FIG. 10 and described herein), but alternative embodiments are contemplated wherein the number, alignment and interconnection of cell regions 20 may be arranged in a hexagonal cellular array, sometimes referred to as a HEXFET.

Formed within P well 29 are two heavily doped N+ implant source regions 31 and 32 on opposing sides of a heavily doped, central implant P+ base 33, as shown. N+ implant source regions 31 and 32 are heavily doped with N-type impurities to an "N+" concentration, and P+ base 33 is heavily doped with P-type impurities to an "P+" concentration. N+ implants 31 and 32 comprise the two sources of the cell region 10 of MOSFET 21, and P+ base 33 provides ohmic contact to P well 29. The upper surfaces of P+ base 33, of N+ implants 31 and 32, of P well 29 and of CSL epilayer 25 (or of drift layer 24 if there is no

separate CSL epilayer 25) are coplanar and together form the upper surface 28 of substrate body 22.

Referring to FIGS. 3 and 4, FIG. 4 is a view of MOSFET 21 shifted one half cell width laterally from the view of FIG. 3. Formed atop upper substrate surface 28 and centered over the left end 36 of one P well 29 and the right end 37 of an immediately adjacent P well 29 is a polycrystalline silicon (polysilicon) gate 38 that is surrounded along its top, bottom, left and right sides by an insulating layer of silicon dioxide 41. Formed atop P+ base 33 is a Ti/Al contact metal 43, and a Ni contact metal 44 is formed atop Ti/Al contact metal 43. An Ni ohmic contact metal 45 is formed over the entire MOSFET 21, overlapping the polysilicon gate 38, but insulated from it by the thick oxide layer 41 on the top and sides thereof.

Because gate 38 is completely surrounded by insulating oxide layer 41, its positionment relative to source contacts 31 and 32 is much less critical, and it cannot detrimentally come in contact with any portion of the Ni metal contact 45 due to any mask misalignment during processing. Gate 38 is centered over the JFET region 48 defined in CSL epilayer 25 between the facing ends 36 and 37 of adjacent P wells 29. Ni ohmic contact metal 45 extends over and contacts with the MOSFET 21 sources (N+ implants) 31 and 32, as well as Ti/Al and Ni metals 43 and 44, respectively. Once gate 38 and Ti/Al and Ni metals are formed atop surface 28, the deposition of Ni metal contact 45 over the entire MOSFET 21 (which is later followed by selective etching to expose and access one portion of commonly connected gates 38) makes conformal, direct and self-aligning contact with the Ti/Al and Ni metals 43 and 44 and, most importantly, with N-source implants 31 and 32. A Ti/Au layer 53 is then formed atop Ni metal contact 45, and thus over all of Ni metal contact 45.

Referring to FIG. 5, MOSFET 21 is there shown as an intermediate semiconductor product 58 with all substrate, layers and doping fabricated up through top SiC surface 28 (which together constitute substrate body 22), an oxidation layer 59, a 4000 A thick layer 66 of polysilicon formed across oxidation layer 59, and application of gate mask 62 atop polysilicon layer 66 in preparation for etching away polysilicon layer 59 to create gates 38. The fabrication of intermediate semiconductor product 58, as shown in FIG. 5, can be

Petrosky, Carol

From: edison@od.nih.gov
Sent: Monday, February 04, 2008 11:02 AM
To: Petrosky, Carol
Subject: iEdison Invention Disclosure Modified Notification

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I. INTRODUCTION

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II. DISCLOSURE OF INVENTION

A. TITLE:

Brief title that discloses what the invention does. 10 words or less.

SiC Power DMOSFETs with Self-Aligned Source Contacts

B. BRIEF DESCRIPTION OF THE INVENTION:

Describe the invention in concise, simple terms. What does it do? How does it work?

Reduces area of the transistor and eliminates variations due to alignment tolerances.

C. TECHNICAL DESCRIPTION AND SUPPORTING DATA:

This description should allow one skilled in the art to practice the proposed inventions. Describe the best way of practicing invention along with possible modifications and variations on the best way. Do not withhold any key elements of the invention, as a complete description is essential to an enforceable patent. Sketches, drawings, photos, reports and manuscripts will be helpful. **You may attach additional pages as needed.**

Please refer to patent notebook entries (attached).

D. KEYWORDS:
Please list the keywords that would be useful for researching for related references for this invention.

SiC MOSFETs

SiC Power Transistors

E. USES:
Please indicate the primary uses/applications/products of the technology as you perceive it.

Electronic power switching, regulation, and control. Motor drives. Power converters.

F. ADVANTAGE:
Indicate the advantages of this technology over other alternatives.

Reduces transistor area (increasing yield and reducing cost. Reduces variations due to mask misalignments during fabrication.

III. POTENTIAL LICENSEES/COMPETITORS

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Cree, Inc. John Palmour or Anant Agarwal.

B. COMPETITORS:
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C. Have you communicated with any industry representative regarding your inventions?

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City/State/Zip

IV. PUBLIC DISCLOSURE

Public disclosure includes abstracts and presentations at scientific meetings (including poster sessions), public seminars, shelving of theses, publications, disclosure to others outside of the University who have not signed a confidentiality agreement, and the use, sale, or offer of sale of the invention. Identify the first dates and circumstances of any such disclosures. Also indicate your future disclosure or publication plans.

A. Which of the following have you done or do you intend to do?

	YES	NO	DATE	
1. Publish	☑	☐	_____	Public disclosures
2. Thesis	☐	☑	_____	are likely in the
3. Oral Presentation	☑	☐	_____	second half of 2008.
4. Poster Session	☑	☐	_____	
5. Disclose to Industry Rep.	☐	☐	_____	
6. Other Public Disclosure	☐	☐	_____	
7. Date of Conception			Spring 2006	

B. Please provide any published technical material such as patents, commercial literature, or scientific articles relating to the invention.

None

V. SPONSORED FUNDING

The primary purpose of this section is to identify any specific grant or contract number(s) (not Purdue account numbers) and the external sponsors (government agencies, industrial sponsors, private agencies, or others) which provided support used to defray costs related to the research from which the invention resulted. This information is required by federal law and is needed to determine whether this invention is subject to any commitments or restrictions arising from the terms of sponsorship.

A. Please provide the following information for EACH contract and grant support.

Funding Agency 1: DARPA
Grant/Contract #: N00014-05-1-0437
Purdue Reference #: _____
} conception

Funding Agency 2: U.S. Army TACOM
Grant/Contract #: W56HZV-06-C-0028
Purdue Reference #: _____
} reduction to practice

Funding Agency 3: _____
Grant/Contract #: _____
Purdue Reference #: _____

VI. INDENTIFICATION OF CONTRIBUTOR(S)

A. PURDUE CONTRIBUTORS:

List below all Purdue persons who are believed to have contributed to the conception or reduction to practice of this invention. Make additional copies as needed.

Contributor #1

First Name: James Middle Name: Albert Last Name: Cooper
Dept/Center Affiliation: 1. ECE *Appointment %: 100
(List all) 2. *Appointment %:
3. *Appointment %:

* Information necessary to apportion Department share of Royalties.

Campus Email: cooperj@purdue.edu Phone: (b) (6)
Home Address: (b) (6)
City/State/Zip:
Home Email: (none) Phone: (b) (6)

**US Citizen: ☑ Resident Alien: ☐ Non-Resident Alien: ☐
Country of Residency:
Country of Citizenship:

** Information necessary for filing patent applications with the USPTO

Contributor #2

First Name: [redacted] Middle Name: Last Name: [redacted]
Dept/Center Affiliation: 1. [redacted] *Appointment %: [redacted]
(List all) 2. *Appointment %:
3. *Appointment %:

* Information necessary to apportion Department share of Royalties.

Campus Email: Phone:
Home Address: [redacted]
City/State/Zip:
Home Email: [redacted] Phone:

**US Citizen: ☐ Resident Alien: [redacted] Non-Resident Alien: ☐
Country of Residency: [redacted]
Country of Citizenship: [redacted]

** Information necessary for filing document with the USPTO

B. NON-PURDUE CONTRIBUTORS

List any non-Purdue individuals who may have worked on either the conception or reduction to practice of this invention.

Non-Purdue Contributor

First Name: Asmita Middle Name: Last Name: Saha
Company Name: Intel
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(Dr. Saha was an employee of Purdue ECE at the time of the invention.)

VII. INVENTION ASSIGNMENT AND CONTRIBUTION CREDIT

I (We) acknowledge and agree that this disclosure is made pursuant to and controlled by the provisions of Purdue University Policy VIII.4.1. To the full extent of my (our) right(s) as inventor(s) of the Invention, by signing this document I (we) acknowledge that the Invention and all patent ownership and other legal rights relating thereto are unconditionally assigned to Purdue University (and/or its designee Purdue Research Foundation, at the option of Purdue University) for all purposes.

List as inventors those individuals who, individually or jointly, contributed either to the conception or reduction to practice of your invention. In the event that Purdue University (or its designee) files a patent application relating to your disclosure, actual inventorship will be determined as a matter of law by a patent attorney. Do not list any inventor gratuitously. Use your full legal name, including middle name, please sign below and then print: Prof./Dr./Mr./Ms., followed by your full legal name.

I (We) propose to divide any Invention proceeds that are shared with the listed inventor(s) in the proportion(s) specified before each signature below.

Percentage %	Inventor/ Contributor Signature	(Print): Title Full Legal Name	Date
50	(b) (6)	PROFESSOR JAMES ALBERT COOPER, JR	1/9/08
50		DR. ASMITA SAHA	

If you have any questions, please call 765-494-5784